

¹ AUTOMATIC DESIGN OF DIGITAL

sck ss mosi miso An

IO Description

XXXX_XXXX XXXX_XXX

1 0 0011_1100 1001_101

Gatelevel Netlist

g301(.A (n 7), .Y (n 4))

Cadence Genus(TM) Synthesis Solution 21.10-p002_1 : Jan 6 2024 00:51:27 GMT (Jan 6 2024 00:51:27 UTC

_3, n_4, n_5, n_6, n_7, n_8;

Grammar

expression)

(assign)

(expression) * (expression)

 $| input | \langle c \rangle | \langle x \rangle$

(c) ::= c0 | c1 | c2 | c3

Logic Synthesis

[emperature (Celsius)

Core Voltage (Volts)

IO Voltage (Volts)

Total Power (in Milliwatt)

Datapath Delay (in Pico Second) 1691 5180

Transform the high-level

6562

6568

17.60

6513

14.40

 $\langle \mathbf{x} \rangle ::= \mathbf{x} \mathbf{1} | \mathbf{x} \mathbf{2} | \mathbf{x} \mathbf{3}$

A grammar specifies the subset of a Hardware

Description Language

CIRCUITS

Design Specification

Architecture Description

descriptions.

Place-and-Route (PnR)

Use Machine Learning to

circuits from high level

automatically design digital





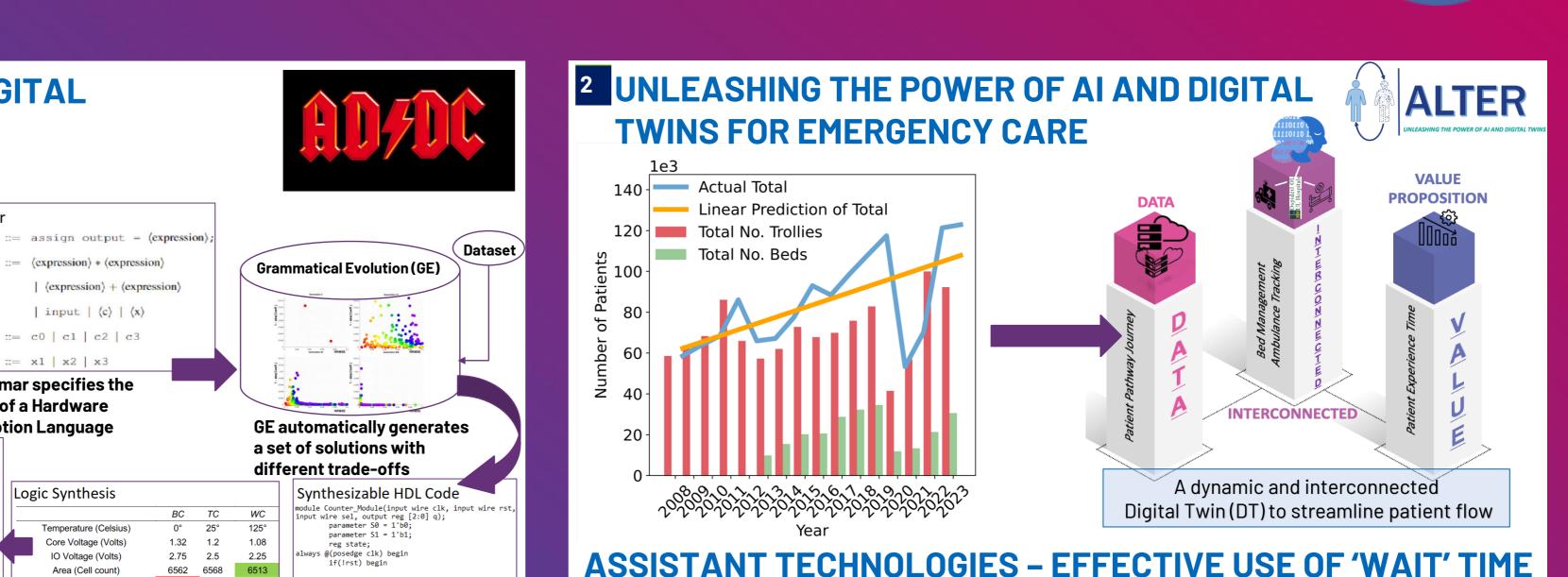
Biocomputing and Developmental Systems (BDS) Group

if(!rst) begin

if (sel == S1) begin

state <= 0 + sel;</pre>

q <= q - 1;

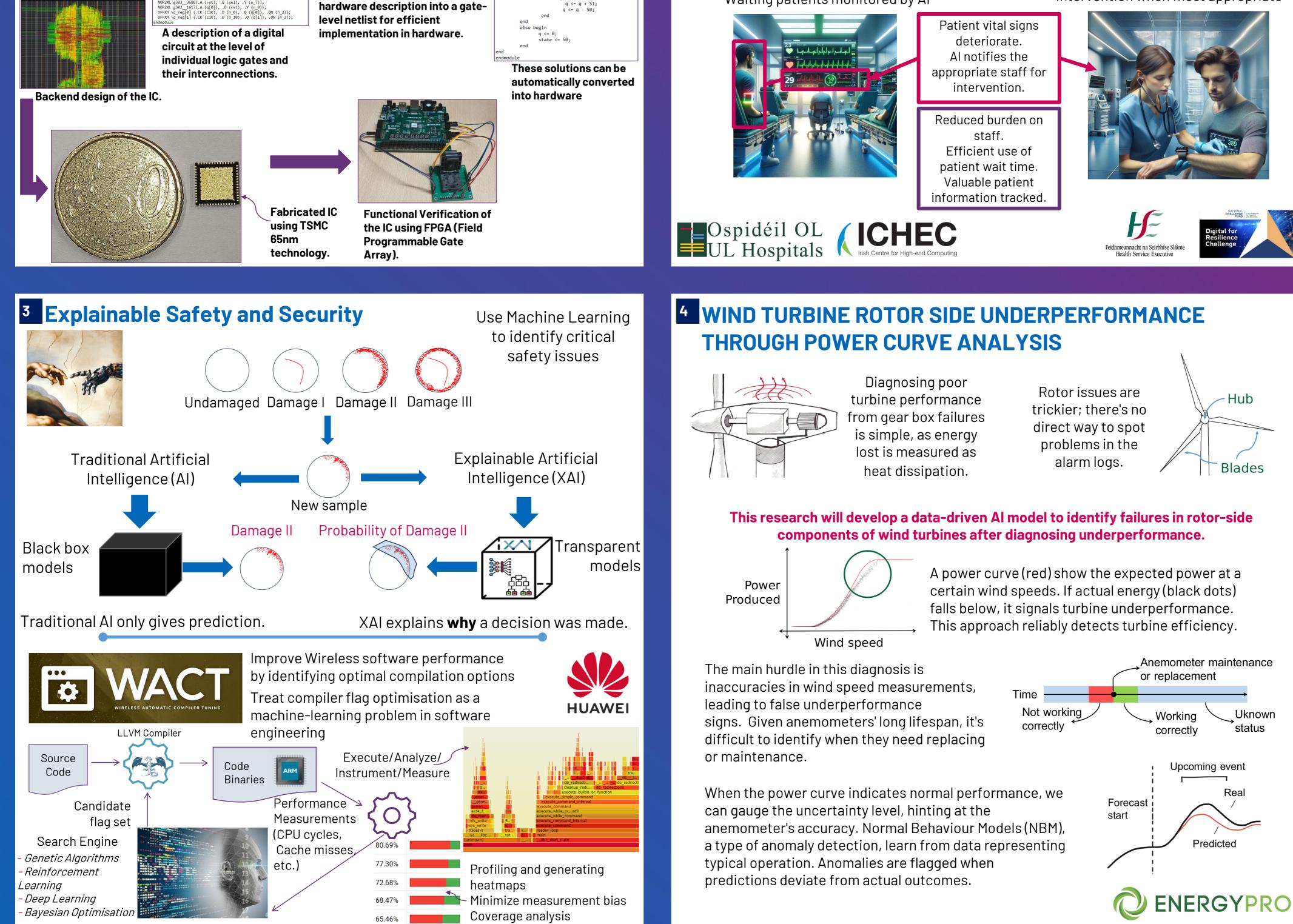


Waiting patients monitored by AI

Intervention when most appropriate

Science

Ireland For what's next



HOST INSTITUTION



